AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

Claims 1-18 (Canceled).

19. (Previously presented) An electronic system, comprising:

at least one input/output device; and

an integrated circuit, coupled to the at least one input/output device, and comprising

functional circuitry for executing logical operations upon digital data signals in a synchronous fashion; and

access circuitry coupled to said functional circuitry and further coupled to a memory core in said integrated circuit for asynchronously accessing said memory core more than once in a single clock cycle.

20. (Previously presented) The electronic system of Claim 19, wherein said electronic system is a cellular telephone.

21. (Previously presented) The electronic system of Claim 19, wherein said memory core is part of a dual-access RAM.

22. (Previously presented) The electronic system of Claim 19, wherein said memory core and said access circuitry combine to form a multiple access memory core.

23. (Previously presented) The electronic system of Claim 19, wherein said access circuitry is embodied in an electronic device coupling a memory interface unit to said memory core.

24. (Previously presented) The electronic system of Claim 19, wherein said electronic system is a digital signal processor.

25. (Previously presented) The electronic system of Claim 19, wherein said memory core is part of a core of a processor.

26. (Previously presented) The electronic system of Claim 19, wherein addresses accessed in said memory core are adjacent addresses.

27. (Previously presented) The electronic system of Claim 19, wherein addresses accessed in said memory core are non-adjacent addresses.

28. (Previously presented) An electronic system, comprising:

at least one input/output device; and

an integrated circuit, coupled to the at least one input/output device, and comprising:

functional circuitry for executing logical operations upon digital data signals in a synchronous fashion; and

access circuitry coupled to a memory core in said integrated circuit for accessing said memory core more than once in a single clock cycle wherein self-timing logic provides signals that facilitate said accessing.

29. (Previously presented) The electronic system of Claim 28, wherein said electronic system is a cellular telephone.

30. (Previously presented) The electronic system of Claim 28, wherein said memory core is part of a dual-access RAM.

31. (Currently amended) The electronic system of Claim 28, wherein said memory core and said access circuitry combine to form a multiple access memory core.

32. (Previously presented) The electronic system of Claim 28, wherein said access circuitry is embodied in an electronic device coupling a memory interface unit to said memory core.

33. (Previously presented) The electronic system of Claim 28, wherein said electronic system is a digital signal processor.

34. (Previously presented) The electronic system of Claim 28, wherein said memory core is part of a core of a processor.

35. (Previously presented) The electronic system of Claim 28, wherein addresses accessed in said memory core are adjacent addresses.

36. (Previously presented) The electronic system of Claim 28, wherein address accessed in said memory core are non-adjacent addresses.

37. (Previously presented) A memory module, comprising:

a memory interface unit;

a memory core; and

circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle.

38. (Previously presented) A memory module, comprising:

a memory interface unit;

a memory core; and

circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle, said circuitry comprising a multiplexer having a first input coupled to a first address bus, a second input coupled to receive a second address bus, an output coupled to an input of said memory core; and logic circuitry having an input coupled to receive an output signal from said memory core and an output coupled to an input of said multiplexer.

39. (Currently amended) The memory module of Claim 38, wherein an output signal from said memory core is a signal that indicates that ~~the~~ a hold time on one of said first and second address busses is achieved.

40. (Previously presented) The memory module of Claim 38, wherein an output signal from said memory core is a signal that indicates that a hold time on one of said first and second address busses is achieved and that it is possible to present a new address on the bus.

41. (Previously presented) The memory module of Claim 38, wherein said logic circuitry is self-timing.

42. (Previously presented) The memory module of Claim 41, wherein said self-timing logic circuitry is used for addressing and for switching data that must be written in said memory core.

43. (Previously presented) The memory module of Claim 41, wherein said self-timing logic circuitry facilitates a dissociation between what is clocked on a system clock and access to the memory core.

44. (Previously presented) A memory module, comprising:

a memory interface unit;

a single-access memory core; and

circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle.

45. (Previously presented) A memory module, comprising:

a memory interface unit;

a memory core; and

circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle, said circuitry comprising a multiplexer having a first input coupled to a first address bus, a second input coupled to receive a second address bus, an output coupled to an input of said memory core; and delay circuitry having an input coupled to receive a signal for input to said memory core and an output coupled to an input of said multiplexer.

46. (Previously presented) The memory module of Claim 45, wherein said signal for input to said memory core is a strobe signal.

47. (Previously presented) A memory module, comprising:

a memory interface unit;

a memory core; and

circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle, wherein an address bus, a data in bus, a data out bus, a first signal line for an access ready signal, a second signal line for an output ready signal, and at least two signal lines for strobe signals couple said circuitry to said memory core.

48. (Previously presented) A memory module, comprising:

a memory interface unit;

a memory core; and

circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle, wherein a memory module is accessed by a first bus and a second bus while addresses of a third bus and a fourth bus are temporarily dispatched to said memory core.

49. (Previously presented) A memory module, comprising:

a memory interface unit;

a memory core; and

circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle, wherein a first bus address is switched using a signal from a system clock while a second address bus is switched using a signal other than from said system clock.

50. (Previously presented) The memory module of Claim 37, wherein addresses accessed in said memory core are adjacent addresses.

51. (Previously presented) The memory module system of Claim 37, wherein address accessed in said memory core are non-adjacent addresses.

52. (Previously presented) A processing apparatus, comprising:

a processing engine; and

a processor backplane coupled to said processing engine, said processor backplane comprising a memory module, said memory module, comprising:

a memory interface unit;

a memory core; and

circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle.

53. (Previously presented) The processor backplane of Claim 52, wherein a bus couples said memory module to said processing engine.

54. (Previously presented) The processing apparatus of Claim 52, wherein said processor backplane further comprises a memory cache coupled to said processing engine.

55. (Previously presented) The processing apparatus of Claim 52, wherein said processor backplane further comprises at least one peripheral device coupled to said processing engine.

56. (Previously presented) The processing apparatus of Claim 52, wherein said processor backplane further comprises an external interface coupled to said processing engine.

57. (Previously presented) The processing apparatus of Claim 52, wherein said processing engine comprises a processing core coupled to a memory management unit.

58. (Previously presented) The processing apparatus of Claim 57, wherein said processing core is a central processing unit.

59. (Previously presented) The processing apparatus of Claim 57, wherein said processing core comprises:

an instruction buffer unit;

a program flow unit;

an address data flow unit; and

a data computation unit coupled to said instruction buffer unit, said program flow unit and said address flow unit.

60. (Previously presented) The processing apparatus system of Claim 52, wherein addresses accessed in said memory core are adjacent addresses.

61. (Previously presented) The processing apparatus of Claim 52, wherein addresses accessed in said memory core are non-adjacent addresses.

62. (Previously presented) The memory module of Claim 37, wherein said circuitry is in other than said memory interface unit.

63. (Previously presented) The processing apparatus of Claim 52, wherein said circuitry is in other than said memory interface unit.